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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/967,240	09/28/2001	Sanu K. Mathew	884.448US1	6550

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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2193	

DATE MAILED: 06/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/967,240	MATHEW ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment filed 03/04/2005.

2. Claims 1-37 are pending in this application. Claims 1, 8, 22, 28, and 33 are independent claims. In Amendment, claims 1, 8, 22, 28, and 33 are amended. This Office Action is made final.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-37 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re claim 1, li mitation "in parallel" is indefinite in lines 7 and 10 because the second circuit is not operated in parallel with the first circuit as cited in line 7, but rather the second circuit is using the output of the first circuit for operating. Similarly, the sum generator is not operated in parallel with the first circuit and the second circuit as cited in line 10, but rather the sum generator is using the output of the second circuit for selecting final results as seen in Figure 1 of the present invention. For examination purposes, the examiner disregards the limitation "in parallel" in lines 7 and 10. Claims 8, 22, 28, and 33 have the same rejection.

Thus, claims 2-7, 9-21, 23-27, 29-32, and 34-37 are also rejected for being dependent on the rejected base claims 1, 8, 22, 28, and 33 respectively.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 7-10, 12, 16, 21-30, 32-34, and 36-37 are rejected under 35 U.S.C. 102(b) as being anticipated by Goto et al. (U.S. 5,047,976).

Re claim 1, Goto et al. disclose in Figure 11 an adder (e.g. col. 11 lines 49-50) to sum two binary numbers, comprising: a first circuit (e.g. all MPX4 and MPX3 with label 46-47) having a plurality of carry-merge stages (e.g. two stage wherein the first stage is MPX4 and the second stage is MPX3) connected in a series (e.g. MPX3 is connected to MPX4), the first circuit adapted to generate a group of carries (e.g. each output of MPX4 or MPX3), the group of caries including a final carry generated by a final stage of the series (e.g. C23 of MPX3), a first carry generated by a first stage of the series (e.g. C7 of MPX4) and a second carry generated by one of the plurality of stages of the series located between the first and final stages of the series (e.g. C15 of MPX3); a second circuit (e.g. all the MXP3 beside MPX3 46-47) operating in parallel with the first circuit and having a plurality of stages (e.g. MPX3 49 is connect to MPX3 48), the second circuit connected to receive the final carry (e.g. C23 from/to MPX3) and the second carry (e.g. C15 into

MPX3 48) and adapted to produce a pair of conditional carry (e.g. output of MPX 48 as C27*(1) and C27*(0)); at least one sum generator (e.g. 11-41 conditionally) operating in parallel with the first circuit and the second circuit and connected to receive the first carry (e.g. for generating F12-F15 using MPX3 46) and one of the pair of conditional carry the sum generator adapted to generate a pair of conditional sums (e.g. all of MPX3 beside MPX3 46-47); and at least one device adapted (e.g. the mux 46-51) to select between the pair of conditional sums (e.g. F12-F43) in response to one of the group of carries (e.g. control carry signal into each MPX3).

Re claim 7, Goto et al. further disclose in Figure 11 the at least one circuit is a sparse carry-merge circuit (e.g. first circuit is considered as sparse carry-merge circuit).

Re claim 8, Goto et al. disclose in Figure 11 an adder (e.g. col. 11 lines 49-50) to sum two binary numbers, comprising: a sparse carry-merge circuit (e.g. all MPX4 and MPX3 with label 46-47) adapted to generate a first predetermined number of carry signals (e.g. C7, C15, C23), the carry signals including a final carry signal generated by a final merge-carry stage (e.g. C23) of the sparse carry-merge circuit, a first carry signal generated by a first stage (e.g. C7) of the sparse carry-merge circuit, and a second carry signal generated by one of a plurality of merge-carry stages connected in series between the first and final stages of the series (e.g. C15) in the sparse carry-merge circuit; a plurality of intermediate carry generators (e.g. other MPX3 beside MPX3 46-47) each coupled to the sparse carry merge circuit (e.g. all MPX4 and MPX3 with label 46-47) and adapted to receive the final carry signal (e.g. C23) and the second carry signal (e.g. C15) and adapted to generate a second predetermined number of carry signals including of a

first and a second intermediate conditional carry signal (e.g. C27*(1) and C27*(0) out from MPX3 48), plurality of selection circuits (e.g. all the MPX3) connected to the plurality of intermediate carry generators and adapted to select between one of a first and a second intermediate conditional carry signals (e.g. 48); and a plurality of conditional sum generators (e.g. F24(1)-F27(1) and F24(0)-F27(0) into 48) coupled to receive the first carry signal (e.g. for MPX 46) and the one of the first and the second intermediate conditional carry signals from the sparse carry-merge circuit and the plurality of selection circuits and adapted to provide the a conditional sum (e.g. output of each MPX3) of the two binary numbers.

Re claim 9, Goto et al. further disclose in Figure 11 the sparse carry-merge circuit merges groups of sixteen bits of the two binary numbers and the first predetermined number of carry signals is one carry signal from each group (e.g. same structure would apply for different grouping).

Re claim 10, Goto et al. further disclose in Figure 11 the sparse carry-merge circuit merges groups of eight bits of the two binary numbers and the first predetermined number of carry signals is one carry signal from each group (e.g. same structure would apply for different grouping).

Re claim 12, Goto et al. further disclose in Figure 11 the sparse-carry merge circuit includes a the plurality of stages, each stage including a plurality of carry-merge logic gates to combine adjacent output signals from a preceding stage to provide the first predetermined number of carry signals (e.g. MPX4 42 combine C7(1) and C7(0) with C3 to yield C7).

Re claim 16, Goto et al. further disclose in Figure 11 each of the plurality of intermediate carry generators (e.g. carry output from CSA 32-41) comprises a plurality of rail pairs, one rail of each rail pair being adapted to generate a first conditional carry signal for a logic 0 carry being input to the intermediate carry generator (e.g. C7(0)) and another rail of each rail pair being adapted to generate a second conditional carry signal for a logic 1 carry being input to the intermediate carry generator (e.g. C7(1)).

Re claim 21, Goto et al. further disclose in Figure 11 a multiplexer (e.g. MPX3 48) recovery circuit coupled to the sparse carry-merge circuit (e.g. part of carry-merge circuit is output of 37), each of the plurality of intermediate carry generators (e.g. C15) and each of the plurality of conditional sum generators (e.g. output of MPX3 47).

Re claim 22, it is a system claim of claim 8. Thus, claim 22 is also rejected under the same rationale as cited in the rejection of rejected claim 8.

Re claim 23, it is a system claim of claim 9. Thus, claim 23 is also rejected under the same rationale as cited in the rejection of rejected claim 9.

Re claim 24, it is a system claim of claim 10. Thus, claim 24 is also rejected under the same rationale as cited in the rejection of rejected claim 10.

Re claim 25, Goto et al. further disclose in Figure 11 the intermediate carry generator generates at least one carry signal for every group of four input bits to the adder (e.g. C3, C7, C11...).

Re claim 26, Goto et al. further disclose in Figure 11 each of the sum generators comprises: four dual rail sum circuits (e.g. F12(1)-F15(1) and F12(0)-F15(0)), each circuit providing one bit of a final sum and one rail generating a conditional sum for a

logic 0 carry-in and the other rail generating a conditional sum for a logic 1 carry-in; and a multiplexer coupled to each dual rail sum circuit to select the one or the other rail in response to a one in four carry from the intermediate carry generator.

Re claim 27, it is a system claim of claim 21. Thus, claim 27 is also rejected under the same rationale as cited in the rejection of rejected claim 21.

Re claim 28, it is a method claim of claim 26. Thus, claim 28 is also rejected under the same rationale as cited in the rejection of rejected claim 26.

Re claim 29, it has limitation as cited in claim 9. Thus, claim 29 is also rejected under the same rationale as cited in the rejection of rejected claim 9.

Re claim 30, it has limitation as cited in claim 10. Thus, claim 30 is also rejected under the same rationale as cited in the rejection of rejected claim 10.

Re claim 32, Goto et al. further disclose in Figure 11 recovering any erroneously discharged ones of the second predetermined number of carries or digits of the final sum (e.g. output of all MPX3).

Re claim 33, it is a method claim of claim 8. Thus, claim 33 is also rejected under the same rationale as cited in the rejection of rejected claim 8.

Re claim 34, Goto et al. further disclose in Figure 11 forming the sparse carry-merge circuit comprises forming a plurality of stages, each stage including a plurality of carry-merge logic gates to combine adjacent outputs from a preceding stage to provide the group of carries (e.g. output of C7).

Re claim 36, it has limitation as cited in claim 26. Thus, claim 36 is also rejected under the same rationale as cited in the rejection of rejected claim 26.

Re claim 37, it is a method claim of claim 21. Thus, claim 37 is also rejected under the same rationale as cited in the rejection of rejected claim 21.

Allowable Subject Matter

7. Claims 2-6, 11, 13-15, 17-20, 31, and 35 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Response to Arguments

8. Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

May 17, 2005

TODD INGBERG
PRIMARY EXAMINER